AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) A process for synchronizing a clock signal to a data stream, comprising the steps of:

generating a reference signal;

<u>identifying a packet in the data stream as a token packet according to a universal serial bus (USB) protocol by comparing a plurality of intervals in a wave representing bit value changes in the packet;</u>

generating a digital value equal to a number of cycles of the reference signal in a time duration covering a predetermined number of bit periods in [[a]] <u>the token</u> packet in the data stream; <u>and</u>

generating a clock signal synchronized with the data stream by calculating a number of cycles of the reference signal in a bit period of the data stream from the digital value and the predetermined number.

2. (Original) The process of claim 1, the step of generating a reference signal including generating an oscillation signal using a resistor-capacitor oscillator.

3. (Original) The process of claim 1, the step of generating a digital value including generating the digital value equal to the number of cycles of the reference signal in the time duration covering eight bit periods in the packet in the data stream.

4. (Original) The process of claim 3, the step of generating a digital value including generating the digital value equal to the number of cycles of the reference signal in the time duration from a beginning of second bit to a beginning of tenth bit in the packet in the data stream.

5. (Cancelled)

6. (Currently amended) The process of claim 1[[5]], the step of identifying the packet as a token packet including the step of analyzing first ten bits of the packet.

7. (Original) The process of claim 6, the step of analyzing first ten bits of the packet including analyzing a voltage level at a USB data transmission line.

8. (Cancelled)

9. (Currently amended) The process of claim [[8]]1, the step of comparing a plurality of intervals in a wave including the steps of:

verifying whether an interval between a first edge of a first type and a second edge of a second type is approximately equal to an interval between the second edge of the second type and a second edge of the first type;

verifying whether an interval between the first edge of the first type and the second edge of the first type is approximately equal to an interval between the second edge of the first type and a third edge of the first type; and

verifying whether an interval between the first edge of the first type and the third edge of the first type is approximately equal to an interval between the third edge of the first type and a fourth edge of the first type.

10. (Original) The process of claim 9, wherein two time intervals being approximately equal to each other includes the two time intervals having a difference there between less than ten percent thereof.

11. (Currently Amended) ~~The process of claim 1,~~ A process for synchronizing a clock signal to a data stream, comprising the steps of:

generating a reference signal;

generating a digital value equal to a number of cycles of the reference signal in a time duration covering a predetermined number of bit periods in a packet in the data stream; and

generating a clock signal synchronized with the data stream by calculating a number of cycles of the reference signal in a bit period of the data stream from the digital value and the predetermined number, wherein the step of generating a clock signal ~~including~~ includes the steps of:

setting a count to zero;

detecting a change in a bit value in the data stream;

in response to a change in the bit value:

generating a first edge for a cycle of the clock signal; and

setting the count to zero;

in response to no change in the bit value:

increasing the count by one;

in response to the count being equal to the digital value, setting the count to zero;

in response to the count being equal to an odd multiple of the digital value divided by two times of the predetermined number, generating a second edge for the cycle of the clock signal; and

in response to the count being equal to a multiple of the digital value divided by the predetermined number, generating a third edge for the cycle of the clock signal; and

returning to the step of detecting a change in a bit value.

12. (Original) The process of claim 11, wherein:

the step of generating a first edge for a cycle of the clock signal includes generating a rising edge of the clock signal;

the step of generating a second edge for the cycle of the clock signal includes generating a falling edge of the clock signal; and

the step of generating a third edge for the cycle of the clock signal includes generating a rising edge of the clock signal.

13. (Original) The process of claim 11, the step of detecting a change in a bit value in the data stream including detecting the change in the bit value in a packet following a token packet in the data stream according to a universal serial bus (USB) protocol.

14. (Currently Amended) ~~The process of claim 1,~~ A process for synchronizing a clock signal to a data stream, comprising the steps of:

generating a reference signal;

generating a digital value equal to a number of cycles of the reference signal in a time duration covering a predetermined number of bit periods in a packet in the data stream; and

generating a clock signal synchronized with the data stream by calculating a number of cycles of the reference signal in a bit period of the data stream from the digital value and the predetermined number, wherein the step of generating a clock signal ~~including~~ includes the steps of:

setting a first count and a second count to zero;

detecting a bit value change in the data stream;

in response to detecting the bit value change, generating a first edge of the clock signal and setting the first count and the second count to zero;

in response to not detecting the bit value change:

increasing the first count by one and increasing the second count by one;

in response to the second count being equal to the digital value divided by two times of the predetermined number, generating a second edge of the clock signal;

in response to the first count being equal to a multiple of the digital value divided by the predetermined number, generating a third edge of the clock signal and setting the second count to zero; and

in response to the first count being equal to the digital value, setting the first count and the second count to zero; and

returning to the step of detecting a bit value change.

15. (Original) The process of claim 14, wherein:

the step of generating a first edge of the clock signal includes generating a start edge for a cycle of the clock signal;

the step of generating a second edge of the clock signal includes generating a middle edge for the cycle of the clock signal; and

the step of generating a third edge of the clock signal includes generating an end edge for the cycle of the clock signal.

16. (Original) The process of claim 15, generating an end edge for the cycle of the clock signal further including generating a start edge for a subsequent cycle of the clock signal.

17. (Currently Amended) ~~The process of claim 1,~~ A process for synchronizing a clock signal to a data stream, comprising the steps of:

generating a reference signal;

generating a digital value equal to a number of cycles of the reference signal in a time duration covering a predetermined number of bit periods in a packet in the data stream; and

generating a clock signal synchronized with the data stream by calculating a number of cycles of the reference signal iii a bit period of the data stream from the digital value and the predetermined number, wherein the step of generating a clock signal ~~including~~ includes the steps of:

resetting a count to zero;

detecting a change in a bit value in the data stream;

in response to a change in the bit value:

generating a start edge of the clock signal;

and returning to the step of resetting a count to zero; and

in response to no change in the bit value:

increasing the count by one;

in response to the count being equal to a multiple of the digital value divided by the predetermined number:

generating an end edge of the clock signal;

returning to the step of resetting a count to zero in response to the count being equal to the digital value; and

returning to the step of detecting a change in a bit value;

in response to the count being equal to a multiple of the digital value divided by two times of the predetermined number:

generating a middle edge of the clock signal; and

returning to the step of detecting a change in a bit value; and

returning to the step of detecting a change in a bit value.

18. (Original) The process of claim 17, the step of detecting a change in a bit value in the data stream including detecting the bit value in a subsequent packet following a token packet in the data stream.

19. (Original) The process of claim 17, wherein:

the step of generating a start edge of the clock signal includes generating a rising edge of the clock signal;

the step of generating a middle edge of the clock signal includes generating a falling edge of the clock signal; and

the step of generating an end edge of the clock signal includes generating a rising edge of the clock signal.

20. (Original) The process of claim 17, the step of generating an end edge of the clock signal including generating the end edge for a current cycle of the clock signal and a start edge for a subsequent cycle of the clock signal.

21-22. (Cancelled)

23. (Currently Amended) ~~The clock signal synchronization system (101) of claim 22,~~ A clock signal synchronization system, comprising:

a data input bus;

a reference signal generator configured to generate a fixed frequency signal;

a digital data analyzer coupled to said data input bus and to said reference signal generator, said digital data analyzer being configured to generate a digital value equal to a number of cycles of the fixed frequency signal of said reference signal generator in a time duration covering a predetermined number of bit periods in a packet in a data stream at said data input bus; and

a digital synchronized clock signal generator coupled to said data input bus, to said reference signal generator, and to said digital data analyzer, said digital synchronized clock signal generator being configured to generate a clock signal synchronized to the data stream in response to the digital value of the said digital data analyzer, said digital synchronized clock signal generator including a counter configured to count at a rate equal to a frequency of the fixed frequency signal of said reference signal generator, wherein said digital synchronized clock signal generator[[(105)]] is configured to generate the clock signal by performing a synchronization process including the steps of:

setting a count of said counter [[(106)]] to zero;

detecting a change in a bit value in the data stream;

in response to a change in the bit value:

generating a first edge for a cycle of the clock signal; and

setting the count to zero;

in response to no change in the bit value:

increasing the count by one;

in response to the count being equal to the digital value, setting the count to zero;

in response to the count being equal to an odd multiple of the digital value divided by two times of the predetermined number, generating a second edge for the cycle of the clock signal; and

in response to the count being equal to a multiple of the digital value divided by the predetermined number, generating a third edge for the cycle of the clock signal; and

returning to the step of detecting a change in a bit value.

24. (Currently Amended) ~~The clock signal synchronization system (101) of claim 22,~~ A clock signal synchronization system, comprising:

a data input bus;

a reference signal generator configured to generate a fixed frequency signal;

a digital data analyzer coupled to said data input bus and to said reference signal generator, said digital data analyzer being configured to generate a digital value equal to a number of cycles of the fixed frequency signal of said reference signal generator in a time duration covering a predetermined number of bit periods in a packet in a data stream at said data input bus; and

a digital synchronized clock signal generator coupled to said data input bus, to said reference signal generator, and to said digital data analyzer, said digital synchronized clock signal generator being configured to generate a clock signal synchronized to the data stream in response to the digital value of the said digital data analyzer, said digital synchronized clock signal generator including a counter configured to count at a rate equal to a frequency of the fixed frequency signal of said reference signal generator, wherein said digital synchronized clock signal generator [[(105)]] is configured to generate the clock signal by performing a synchronization process including the steps of:

setting a count of said counter [[(106)]] to zero;

detecting a change in a bit value in the data stream;

in response to a change in the bit value:

generating a start edge of the clock signal; and

returning to the step of setting a count of said counter [[(106)]] to zero; and

in response to no change in the bit value:

increasing the count by one;

in response to the count being equal to a multiple of the digital value divided by the predetermined number:

generating an end edge of the clock signal;

returning to the step of setting a count of said counter [[(106)]] to zero in response to the count being equal to the digital value; and

returning to the step of detecting a change in a bit value in the data stream;

in response to the count being equal to a multiple of the digital value divided by two times of the predetermined number, generating a middle edge of the clock signal; and

returning to the step of detecting a change in a bit value in the data stream.

25. (Currently Amended) ~~The clock signal synchronization system (101) of claim 22,~~ A clock signal synchronization system, comprising:

a data input bus;

a reference signal generator configured to generate a fixed frequency signal;

a digital data analyzer coupled to said data input bus and to said reference signal generator, said digital data analyzer being configured to generate a digital value equal to a number of cycles of the fixed frequency signal of said reference signal generator in a time duration covering a predetermined number of bit periods in a packet in a data stream at said data input bus; and

a digital synchronized clock signal generator coupled to said data input bus, to said reference signal generator, and to said digital data analyzer, said digital synchronized clock signal generator being configured to generate a clock signal synchronized to the data stream in response to the digital value of the said digital data analyzer, said digital synchronized clock signal generator including a first counter configured to count at a rate equal to a frequency of the fixed frequency signal of said

reference signal generator, wherein said digital synchronized clock signal [[(105)]] generator further includes a second counter [[(108)]] and is configured to generate the clock signal by performing a synchronization process including the steps of:

setting a first count of said first counter [[(106)]] to zero;

setting a second count of the second counter [[(108)]] to zero;

detecting a bit value change in the data stream;

in response to detecting the bit value change, generating a first edge of the clock signal and setting the first count and the second count to zero;

in response to not detecting the bit value change:

increasing the first count by one and increasing the second count by one;

in response to the second count being equal to the digital value divided by two times of the predetermined number, generating a second edge of the clock signal;

in response to the first count being equal to a multiple of the digital value divided by the predetermined number, generating a third edge of the clock signal and setting the second count to zero; and

in response to the first count being equal to the digital value, setting the first count and the second count to zero; and

returning to the step of detecting a bit value change.

26. (Cancelled)

27. (Currently Amended) The device [[(100)]] of claim [[26]] 28, wherein said data processing element [[(102)]] is configured to move a cursor on a screen of [[a]] the host ~~computer~~ coupled thereto via a universal serial bus (USB) and [[make]] issue commands to the host ~~computer~~.

28. (Currently Amended) ~~The device (100) of claim 27,~~ A device for receiving data from and transmitting data to a host, comprising:

a data processing element coupled to the host; and

a digital synchronization unit including:

an oscillator;

a digital data analyzer coupled to said data processing element and to said oscillator, said digital data analyzer being configured to generate a control signal having a value equal to a number of cycles of a fixed frequency signal of said oscillator in a time duration covering a predetermined number of bit periods in a packet in the data stream at said data processing element; and

a digital synchronized clock signal generator coupled to said data processing element, to said oscillator, and to said digital data analyzer, said digital synchronized clock signal generator being configured to generate a clock signal synchronized to the data stream in response to the control signal, wherein said digital synchronized clock signal generator [[(105)]] includes a counter [[(106)]] and is configured to generate the clock signal by performing a synchronization process including the steps of:

setting a count of the counter [[(106)]] to zero;

detecting a change in a bit value in the data stream;

in response to a change in the bit value:

generating a first edge for a cycle of the clock signal; and

setting the count to zero;

in response to no change in the bit value:

increasing the count by one;

in response to the count being equal to the value of the control signal, setting the count to zero;

in response to the count being equal to an odd multiple of the value of the control signal divided by two times of the predetermined number, generating a second edge for the cycle of the clock signal; and

in response to the count being equal to a multiple of the value of the control signal divided by the predetermined number, generating a third edge for the cycle of the clock signal; and

returning to the step of detecting a change in a bit value.

29. (Currently Amended) ~~The device (100) of claim 27,~~ A device for receiving data from and transmitting data to a host, comprising:

a data processing element coupled to the host, said data processing element configured to move a cursor on a screen of the host coupled thereto via a universal serial bus (USB) and issue commands to the host; and

a digital synchronization unit including:

an oscillator;

a digital data analyzer coupled to said data processing element and to said oscillator, said digital data analyzer being configured to generate a control signal having a value equal to a number of cycles of a fixed frequency signal of said oscillator in a time duration covering a predetermined number of bit periods in a packet in the data stream at said data processing element; and

a digital synchronized clock signal generator coupled to said data processing element, to said oscillator, and to said digital data analyzer, said digital synchronized clock signal generator being configured to generate a clock signal synchronized to the data stream in response to the control signal, wherein said digital synchronized clock signal generator [[(105)]] includes a counter [[(106)]] and is configured to generate the clock signal by performing a synchronization process including the steps of:

setting a count of the counter [[(106)]] to zero;

detecting a change in a bit value in the data stream;

in response to a change in the bit value:

generating a start edge of the clock signal; and

returning to the step of setting a count of the counter [[(106)]] to zero; and

in response to no change in the bit value:

increasing the count by one;

in response to the count being equal to a multiple of the value of the control signal divided by the predetermined number:

generating an end edge of the clock signal;

returning to the step of setting a count of the counter [[(106)]] to zero in response to the count being equal to the value of the control signal; and

returning to the step of detecting a change in a bit value;

in response to the count being equal to a multiple of the value of the control signal divided by two times of the predetermined number, generating a middle edge of the clock signal; and

returning to the step of detecting a change in a bit value.

30. (Currently Amended) ~~The device (100) of claim 27,~~ <u>A device for receiving data from and transmitting data to a host, comprising:</u>

<u>a data processing element coupled to the host, said data processing element configured to move a cursor on a screen of the host coupled thereto via a universal serial bus (USB) and issue commands to the host; and</u>

<u>a digital synchronization unit including:</u>

<u>an oscillator;</u>

<u>a digital data analyzer coupled to said data processing element and to said oscillator, said digital data analyzer being configured to generate a control signal having a value equal to a number of cycles of a fixed frequency signal of</u>

said oscillator in a time duration covering a predetermined number of bit periods in a packet in the data stream at said data processing element; and

a digital synchronized clock signal generator coupled to said data processing element, to said oscillator, and to said digital data analyzer, said digital synchronized clock signal generator being configured to generate a clock signal synchronized to the data stream in response to the control signal, wherein said digital synchronized clock signal generator [[(105)]] includes a counter [[(106)]] and is configured to generate the clock signal by performing a synchronization process including the steps of:

setting a first count of said first counter [[(106)]] to zero;

setting a second count of the second counter [[(108)]] to zero;

detecting a bit value change in the data stream;

in response to detecting the bit value change:

generating a first edge of the clock signal;

setting the first count of said first counter [[(106)]]; and

setting the second count of the second counter [[(108)]] to zero;

in response to not detecting the bit value change:

increasing the first count of said first counter [[(106)]] by one;

increasing the second count of the second counter [[(108)]] by one;

in response to the second count being equal to the value of the control signal divided by two times of the predetermined number:

generating a second edge of the clock signal;

in response to the first count being equal to a multiple of the value of the control signal divided by the predetermined number:

generating a third edge of the clock signal; and

setting the second count of the second counter [[(108)]] to zero;

in response to the first count being equal to the value of the control signal:

setting the first count of said first counter [[(106)]] to zero; and

setting the second count of the second counter [[(108)]] to zero; and

returning to the step of detecting a bit value change.